2.5-A and 5-A, 35-V_{MAX} VDD FET and IGBT Single-Gate Driver

Check for Samples: UCC27531 , UCC27533, UCC27536 , UCC27537, UCC27538

FEATURES

- Low Cost Gate Driver (offering optimal solution for driving FET and IGBTs)
- Superior Replacement to Discrete Transistor Pair Drive (providing easy interface with controller)
- TTL and CMOS Compatible Input Logic Threshold, (independent of supply voltage)
- Split Output Options Allow for Tuning of Turn-On and Turn-Off Currents
- Inverting and Non-Inverting Input Configurations
- Enable with Fixed TTL Compatible Threshold
- High 2.5-A Source and 2.5-A or 5-A Sink Peak Drive Currents at 18-V VDD
- Wide VDD Range From 10 V up to 35 V
- Input and Enable Pins Capable of Withstanding up to -5-V DC Below Ground
- Output Held Low When Inputs are Floating or During VDD UVLO
- Fast Propagation Delays (17-ns typical)
- Fast Rise and Fall Times (15-ns and 7-ns typical with 1800-pF Load)
- Under Voltage Lockout (UVLO)
- Used as a High-Side or Low-Side Driver (if designed with proper bias and signal isolation)
- Low Cost, Space Saving 5-Pin or 6-Pin DBV (SOT-23) Package Options
- UCC27536 and UCC27537 Pin-to-Pin compatible to TPS2828 and TPS2829
- Operating Temperature Range of -40°C to 140°C

APPLICATIONS

- Switch-Mode Power Supplies
- DC-to-DC Converters
- Solar Inverters, Motor Control, UPS
- HEV and EV Chargers
- Home Appliances
- Renewable Energy Power Conversion
- SiC FET Converters

DESCRIPTION

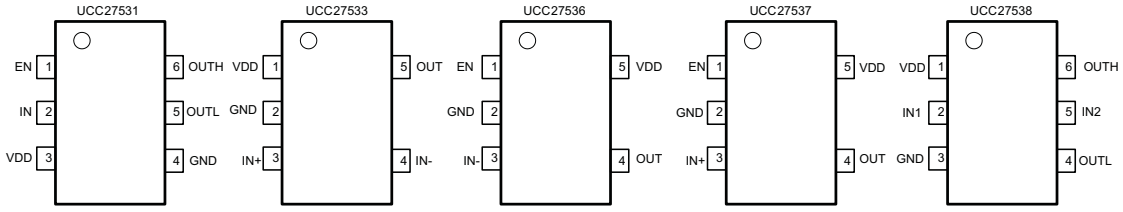
The UCC2753x family of devices are single-channel, high-speed, gate drivers capable of effectively driving MOSFET and IGBT power switches by up to 2.5-A source and 5-A sink (asymmetrical drive) peak current. Strong sink capability in asymmetrical drive boosts immunity against parasitic Miller turn-on effect. The UCC2753x device can also feature a split-output configuration where the gate-drive current is sourced through OUTH pin and sunk through OUTL pin. This pin arrangement allows the user to apply independent turn-on and turn-off resistors to the OUTH and OUTL pins respectively and easily control the switching slew rates.

The driver has rail-to-rail drive capability and extremely small propagation delay typically 17 ns.

The input threshold of UCC2753xDBV is based on TTL and CMOS compatible low-voltage logic, which is fixed and independent of VDD supply voltage. The 1-V typical hysteresis offers excellent noise immunity.

The driver has EN pin with fixed TTL compatible threshold. EN is internally pulled up; pulling EN low disables driver, while leaving it open provides normal operation. The EN pin can be used as an additional input with the same performance as the IN, IN+, IN1, and IN2 pins.

UCC2753x (top view)



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION(CONT.)

Leaving the input pin of driver open holds the output low. The logic behavior of the driver is shown in the application diagram, timing diagram and input and output logic truth table.

Internal circuitry on VDD pin provides an under voltage lockout function that holds output low until VDD supply voltage is within operating range.

The UCC2753x driver is offered in a 5-pin or 6-pin standard SOT-23 (DBV) package. The device operates over wide temperature range of -40°C to 140°C.

ORDERING INFORMATION(1)

PART NUMBER	PACKAGE(2)	PEAK CURRENT (SOURCE AND SINK)	INPUT THRESHOLD LOGIC	OPERATING TEMPERATURE RANGE T_A
UCC27531DBV	SOT-23, 6-PIN	2.5 A and 5 A	TTL/CMOS –Compatible (low-voltage, independent of VDD bias voltage)	-40°C to +140°C
UCC27533DBV	SOT-23, 5-PIN	2.5-A/5-A		
UCC27536DBV	SOT-23, 5-PIN	2.5-A/2.5-A		
UCC27537DBV	SOT-23, 5-PIN	2.5-A/5-A		
UCC27538DBV	SOT-23, 6-PIN	2.5-A/5-A		

(1) DBV package uses Pb-Free lead finish of Pd-Ni-Au which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.
(2) For the most up-to-date packaging information see the TI web site.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range,	VDD	-0.3	35	V
Continuous	OUTH, OUTL, OUT	-0.3	VDD +0.3	
Pulse	OUTH, OUTL, OUT (200 ns)	-2	VDD +0.3	
Continuous IN, EN, IN+, IN-, IN1, IN2		-5	27	V
Pulse IN, EN, IN+, IN-, IN1, IN2 (1.5 µs)		-6.5	27	
Human body model, HBM (ESD)			4000	
Charged device model, CDM (ESD)			1000	
Operating virtual junction temperature range, T_J		-40	150	°C
Storage temperature range, T_{stg}		-65	150	
Lead temperature	Soldering, 10 sec.		300	
	Reflow		260	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

THERMAL INFORMATION

THERMAL METRIC		UCC27533, UCC27536, UCC27537	UCC27531, UCC27538	UNITS
		DBV	DBV(1)	
		5 PINS	6 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	178.3	178.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	109.7	109.7	
θ_{JB}	Junction-to-board thermal resistance(4)	28.3	28.3	
ψ_{JT}	Junction-to-top characterization parameter(5)	14.7	14.7	
ψ_{JB}	Junction-to-board characterization parameter(6)	27.8	27.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, VDD	10	18	32	V
Operating junction temperature range	-40		140	°C
Input voltage, IN, IN+, IN-, IN1, IN2	-5		25	V
Enable, EN	-5		25	

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, VDD = 18 V, $T_A = T_J$ = -40°C to 140°C, 1-µF capacitor from VDD to GND, f = 100 kHz. Currents are positive into, negative out of the specified terminal. OUTH and OUTL are tied together for UCC27531/8. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Bias Currents						
I_{DDoff}	Startup current (UCC25731)	VDD = 7.0, IN, EN=VDD	100	200	300	µA
		IN, EN = GND	100	217	300	
I_{DDoff}	Startup current (UCC27533)	VDD = 7.0, IN+ = GND, IN- = VDD	100	200	300	
		IN+ = VDD, IN- = GND	100	217	300	
I_{DDoff}	Startup current (UCC27536)	VDD = 7.0, IN- = GND, EN = VDD	100	217	300	
		IN- = VDD, EN = GND	100	217	300	
I_{DDoff}	Startup Current (UCC27538)	VDD = 7.0, IN1, IN2=VDD	100	200	300	
		IN1, IN2=GND	100	200	300	
Under Voltage Lockout (UVLO)						
V_{ON}	Supply start threshold		8.0	8.9	9.8	V
V_{OFF}	Minimum operating voltage after supply start		7.3	8.2	9.1	
V_{DD_H}	Supply voltage hysteresis			0.7		
Input (IN, IN+, IN1, IN2)						
V_{IN_H}	Input signal high threshold, output high	Output High, IN- = LOW, EN=HIGH, IN2 or IN1 = HIGH (other is INPUT)	1.8	2.0	2.2	V
V_{IN_L}	Input signal low threshold, output low	Output Low, IN- = LOW, EN=HIGH, IN2 or IN1 = HIGH (other is INPUT)	0.8	1.0	1.2	
V_{IN_HYS}	Input signal hysteresis			1.0		
Input (IN-)						
V_{IN_H}	Input signal high threshold, output low	Output low, IN+ = HIGH, EN = High	1.7	1.9	2.1	V
V_{IN_L}	Input signal low threshold, output high	Output high,, IN+ = HIGH, EN = High	0.8	1.0	1.2	
V_{IN_HYS}	Input signal hysteresis			0.9		
Enable (EN)						
V_{EN_H}	Enable signal high threshold	Output High	1.7	1.9	2.1	V
V_{EN_L}	Enable signal low threshold	Output Low	0.8	1.0	1.2	
V_{EN_HYS}	Enable signal hysteresis			0.9		

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted, VDD = 18 V, $T_A = T_J$ = -40°C to 140°C, 1-µF capacitor from VDD to GND, f = 100 kHz. Currents are positive into, negative out of the specified terminal. OUTH and OUTL are tied together for UCC27531/8. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Outputs (OUTH/OUTL)						
$I_{SRC/SNK}$	Source peak current (OUTH)/ sink peak current (OUTL)(13)	CLOAD = 0.22 µF, f = 1 kHz		-2.5/+5		A
V_{OH}	OUTH, high voltage	I_{OUTH} = -10 mA	VDD -0.2	VDD - 0.12	VDD - 0.07	V
V_{OL}	OUTL, low voltage	I_{OUTL} = 100 mA		0.065	0.125	V
V_{OL}	OUTL, Low Voltage UCC27536	I_{OUTL} = 100 mA		0.130	0.23	V
R_{OH}	OUTH, pull-up resistance (15)	T_A = 25°C, I_{OUT} = -10 mA	11	12	12.5	Ω
		T_A = -40°C to 140°C, I_{OUT} = -10 mA	7	12	20	Ω
R_{OL}	OUTL, pull-down resistance	T_A = 25°C, I_{OUT} = 100 mA	0.45	0.65	0.85	Ω
		T_A = -40°C to 140°C, I_{OUT} = 100 mA	0.3	0.65	1.25	Ω
R_{OL}	OUTL, pull-down resistance UCC27536	T_A = 25°C, I_{OUT} = 100 mA	0.9	1.3	1.7	Ω
		T_A = -40°C to 140°C, I_{OUT} = 100 mA	0.6	1.3	2.3	Ω
Switching Time						
t_R	Rise time	C_{LOAD} = 1.8 nF		15		ns
t_F	Fall time	C_{LOAD} = 1.8 nF		7		ns
t_F	Fall Time UCC27536DBV	CLOAD = 1.8 nF		10		ns
t_{D1}	Turn-on propagation delay	C_{LOAD} = 1.8 nF, IN, IN+ = 0 V to 5 V		17	26	ns
t_{D2}	Turn-off propagation delay	C_{LOAD} = 1.8 nF, IN, IN+ = 5 V to 0 V		17	26	ns
t_{D3}	Inverting turn-off propagation delay	C_{LOAD} = 1.8 nF, IN- = 0 V to 5 V		17	28	ns
t_{D4}	Inverting turn-on propagation delay	C_{LOAD} = 1.8 nF, IN- = 5 V to 0 V		20	28	ns

Timing Diagram

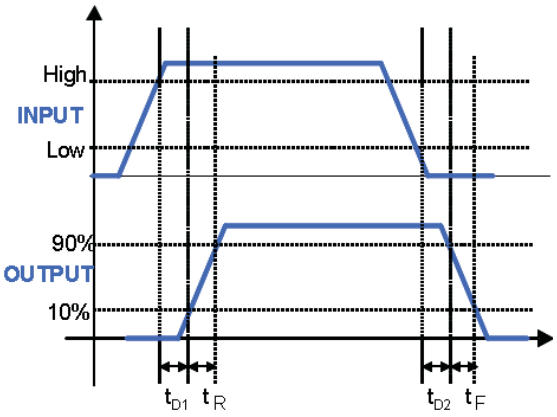


Figure 1.
UCC27531: (OUTPUT = OUTH tied to OUTL) INPUT = IN, (EN = VDD), or INPUT = EN, (IN = VDD)
UCC27537: (OUTPUT = OUT) INPUT = IN+, (EN = VDD), or INPUT = EN, (IN+ = VDD)
UCC27538: (OUTPUT = OUTH tied to OUTL) INPUT = IN1, (IN2 = VDD), or INPUT = IN2, (IN1 = VDD)

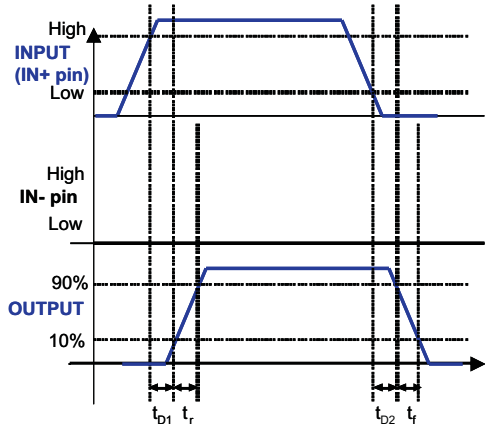


Figure 2. UCC27533: (OUTPUT = OUT) INPUT = IN+
UCC27536: (OUTPUT = OUT) INPUT = EN

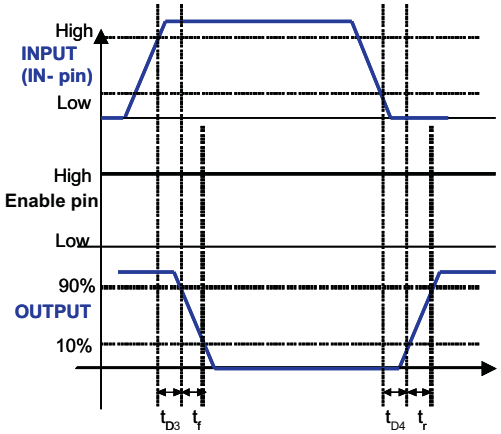


Figure 3. UCC27533: (OUTPUT = OUT) ENABLE = IN+
UCC27536: (OUTPUT = OUT) ENABLE = EN

DEVICE INFORMATION

Block Diagram

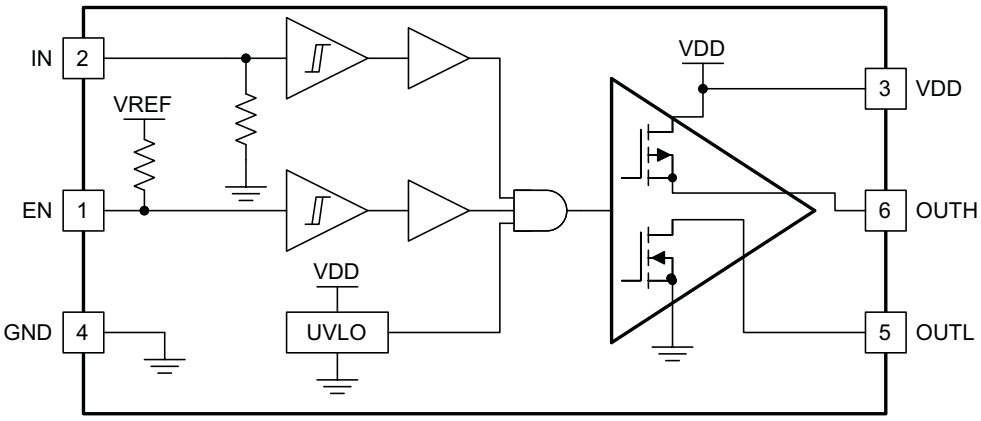


Figure 4. UCC27531
(EN pull-up resistance to VREF = 500 kΩ, VREF = 5.8 V, in pull-down resistance to GND = 230 kΩ)

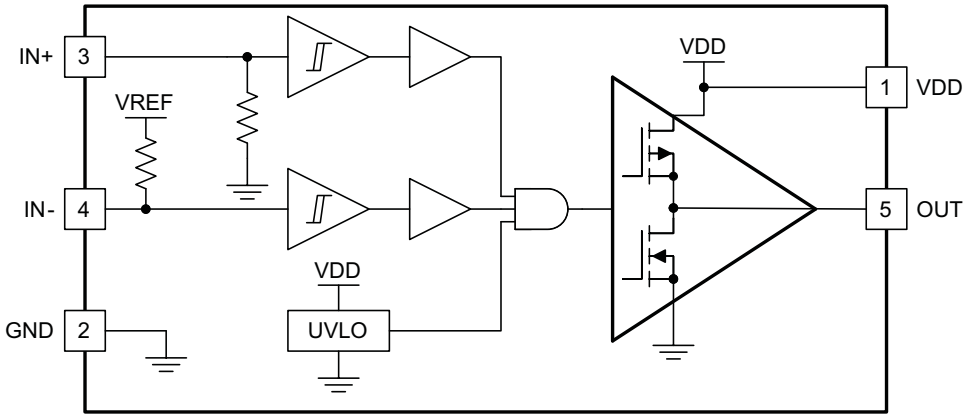


Figure 5. UCC27533
(IN- pull-up resistance to VREF = 500 kΩ, VREF = 5.8 V, IN+ pull-down resistance to GND = 230 kΩ)

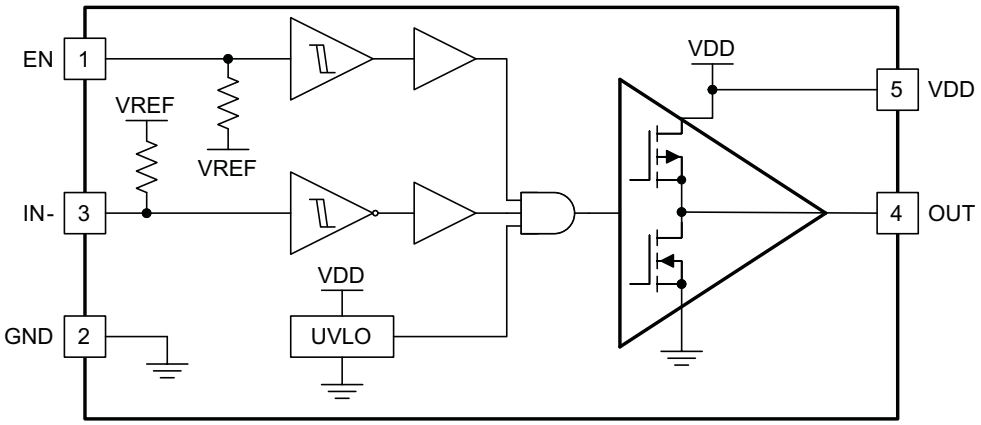


Figure 6. UCC27536
(EN pull-up resistance to VREF = 500 kΩ, VREF = 5.8 V, IN- pull-up resistance to VREF = 500 kΩ)

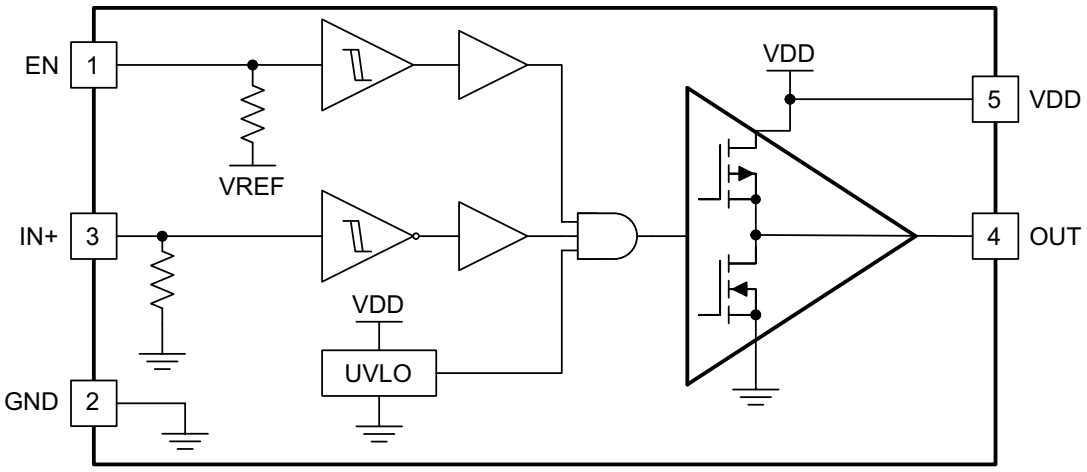


Figure 7. UCC27537
(EN pull-up resistance to VREF = 500 kΩ, VREF = 5.8 V, IN+ pull-down resistance to GND = 230 kΩ)

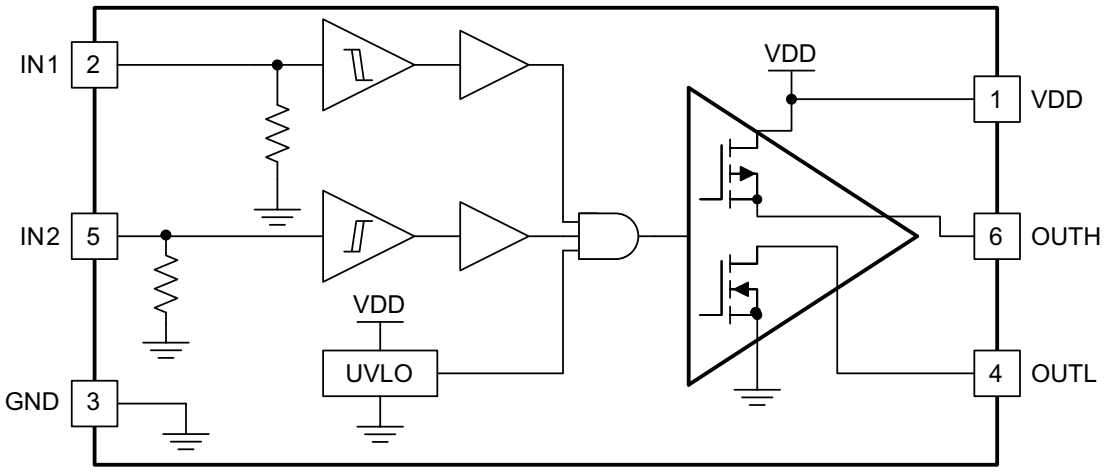


Figure 8. UCC27538
(IN1 pull-down resistance to GND = 230 kΩ, IN2 pull-down resistance to GND = 230 kΩ)

DEVICE INFORMATION

Typical Application Diagrams

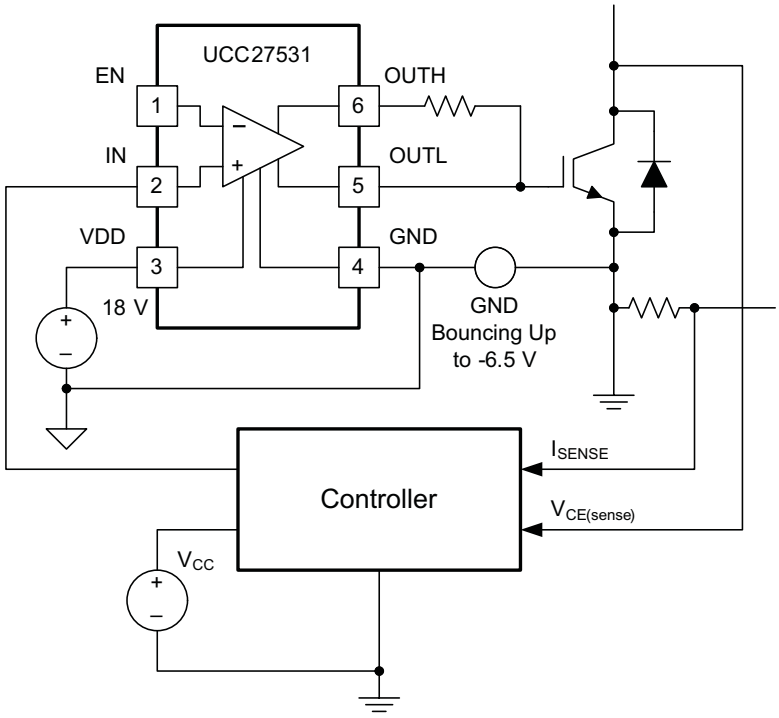


Figure 9. Driving IGBT Without Negative Bias

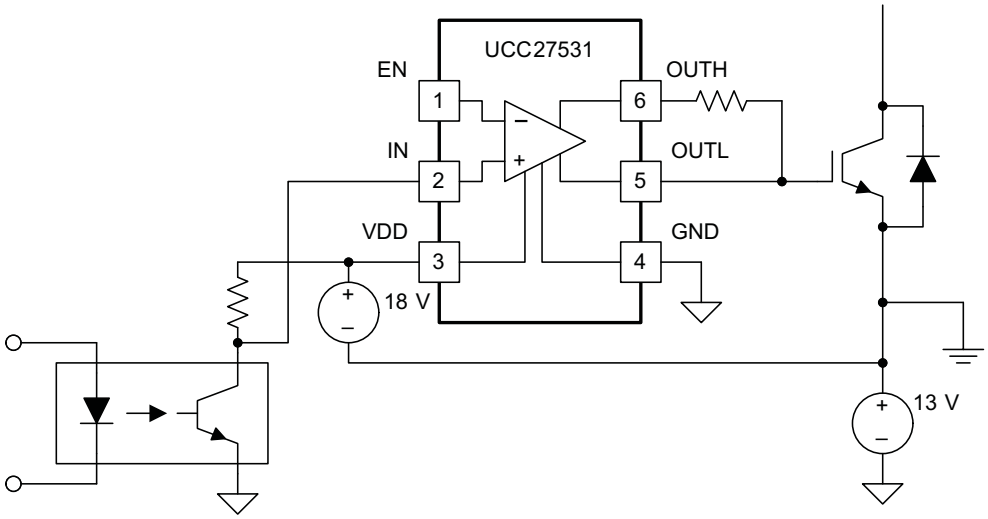


Figure 10. Driving IGBT With 13-V Negative Turn-Off Bias

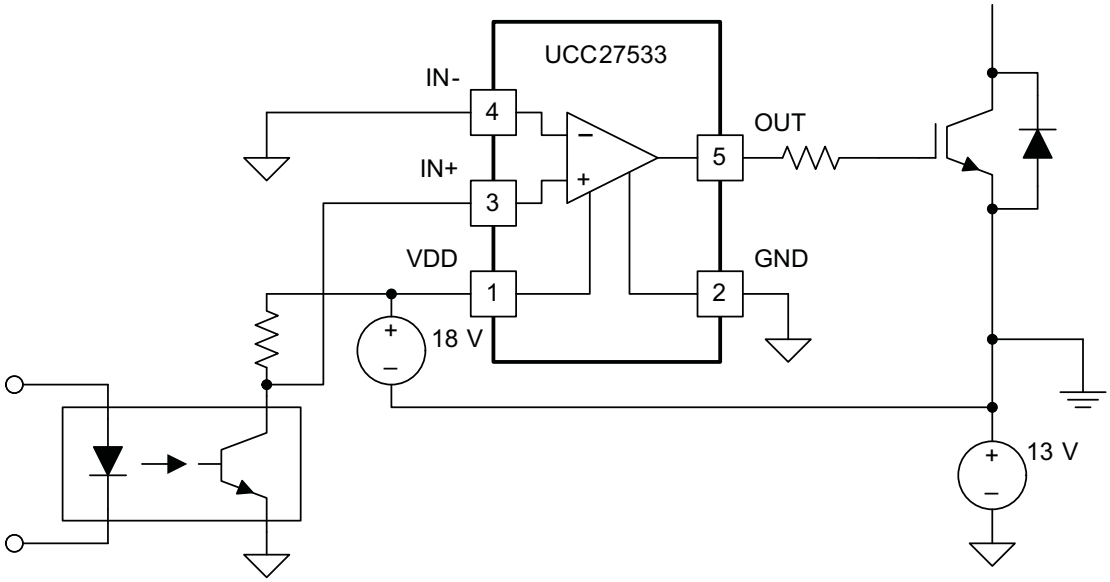


Figure 11. Single Output Driver

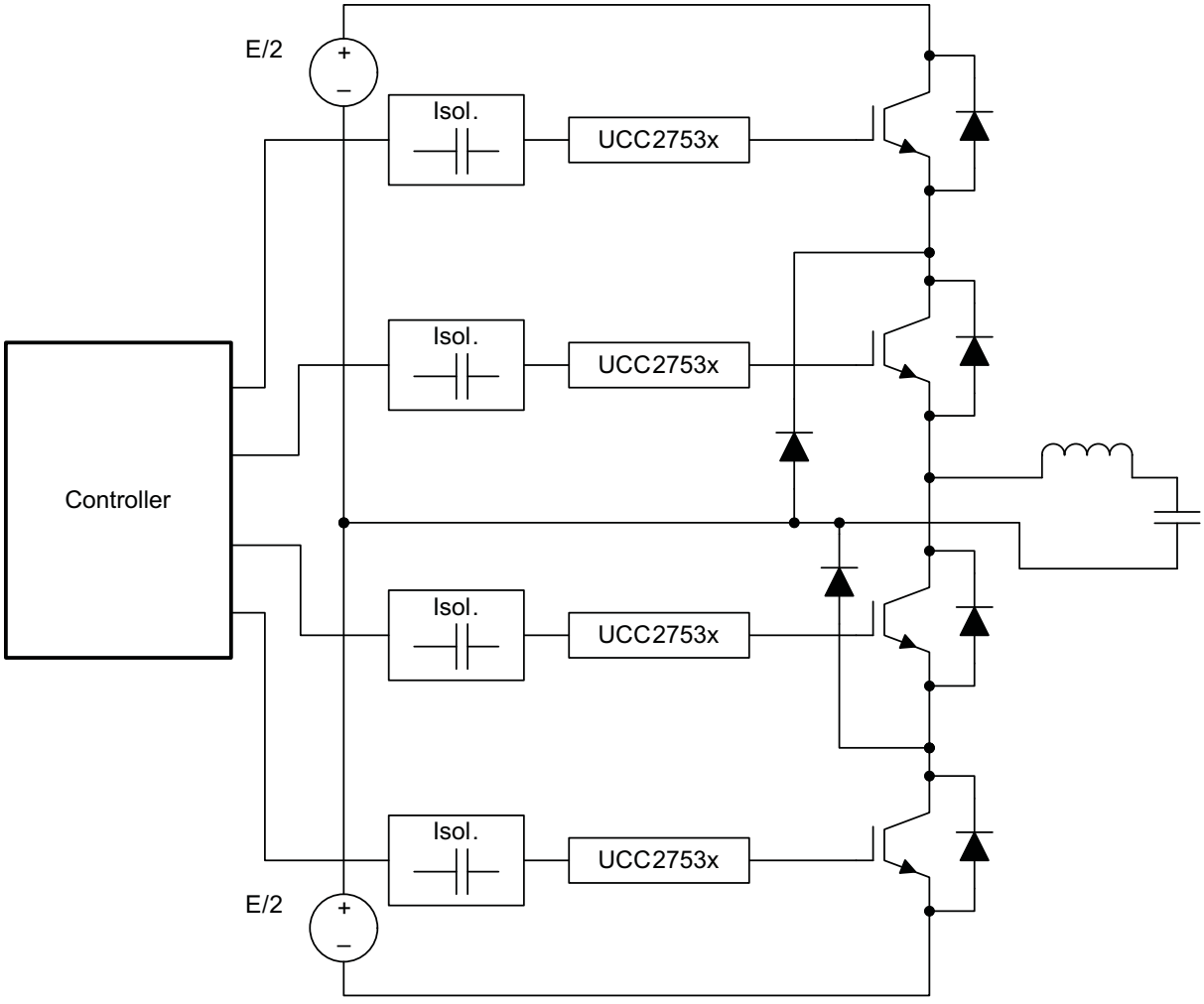
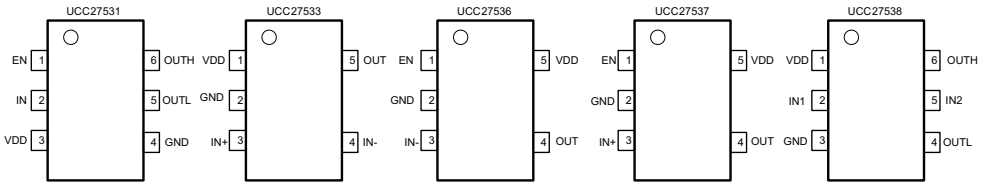


Figure 12. Using UCC2753x Drivers in an Inverter

DEVICE INFORMATION

UCC2753x Product Matrix

Table 1. UCC2753x Product Matrix

	UCC27531	UCC27533	UCC27536	UCC27537	UCC27538
I_{ON} PEAK	2.5 A	2.5 A	2.5 A	2.5 A	2.5 A
I_{OFF} PEAK	5 A	5 A	2.5 A	5 A	5 A
PACKAGE	SOT-23-6	SOT-23-5	SOT-23-5	SOT-23-5	SOT-23-6
IN	Single	Dual	Single	Single	Dual
IN LOGIC	TTL/CMOS	TTL/CMOS	TTL/CMOS	TTL/CMOS	TTL/CMOS
EN	Yes	No	Yes	Yes	No
OUTPUT	Split	Single	Single	Single	Split
INVERTING	No	Inverting/Non-Inverting	Yes	No	No
MAX VDD	35 V	35 V	35 V	35 V	35 V
PIN OUT					

TERMINAL FUNCTIONS

TERMINAL		I/O	FUNCTION
PIN NUMBER	NAME		
UCC27531DBV			
1	EN	I	Enable (Pull EN to GND in order to disable output, pull it high or leave open to enable output)
2	IN	I	Driver non-inverting input
3	VDD	I	Bias supply input
4	GND	-	Ground (all signals are referenced to this node)
5	OUTL	O	5-A sink current output of driver
6	OUTH	O	2.5-A Source Current Output of driver
UCC27533DBV			
1	VDD	I	Bias supply input
2	GND	-	Ground (All signals are referenced to this node)
3	IN+	I	Driver non-inverting input
4	IN-	I	Driver inverting input
5	OUT	O	2.5-A source and 5-A sink current output of driver
UCC27536DBV			
1	EN	I	Enable (pull EN to GND in order to disable output, pull it high or leave open to enable output)
2	GND	-	Ground (all signals are referenced to this node)
3	IN-	I	Driver inverting input
4	OUT	O	2.5-A source and 2.5-A sink current output of driver
5	VDD	I	Bias supply input
UCC27537DBV			
1	EN	I	Enable (Pull EN to GND in order to disable Output, Pull it high or leave open to enable Output)
2	GND	-	Ground (All signals are referenced to this node)
3	IN+	I	Driver non-inverting input
4	OUT	O	2.5-A source and 5-A sink current output of driver
5	VDD	I	Bias supply input
UCC27538DBV			
1	VDD	I	Bias supply input
2	IN1	I	Driver non-inverting input
3	GND	-	Ground (all signals are referenced to this node)
4	OUTL	O	5-A sink current output of driver
5	IN2	I	Driver non-inverting input
6	OUTH	O	2.5-A source current output of driver

INPUT/OUTPUT LOGIC TRUTH TABLE (for single output driver)

UCC27531DBV				
IN PIN	**EN PIN**	**OUTH PIN**	**OUTL PIN**	**OUT (OUTH and OUTL pins tied together)**
L	L	High-impedance	L	L
L	H	High-impedance	L	L
H	L	High-impedance	L	L
H	H	H	High-impedance	H
H	FLOAT	H	High-impedance	H
FLOAT	H	High-impedance	L	L

INPUT/OUTPUT LOGIC TRUTH TABLE

UCC27533DBV		
IN+ PIN	**IN- PIN**	**OUT PIN**
L	L	L
L	H	L
H	L	H
H	H	L
FLOAT	X	L
X	FLOAT	L
UCC27536DBV		
IN- PIN	**EN PIN**	**OUT PIN**
L	L	L
L	H	H
H	L	L
H	H	L
FLOAT	X	L
L	FLOAT	H
UCC27537DBV		
IN+ PIN	**EN PIN**	**OUT PIN**
L	L	L
L	H	L
H	L	L
H	H	H
FLOAT	X	L
H	FLOAT	H

INPUT/OUTPUT LOGIC TRUTH TABLE (for single output driver)

UCC27538DBV				
IN1 PIN	**IN2 PIN**	**OUTH PIN**	**OUTL PIN**	**OUT (OUTH and OUTL pins tied together)**
L	L	High-Impedance	L	L
L	H	High-Impedance	L	L
H	L	High-Impedance	L	L
H	H	H	High-Impedance	H
X	FLOAT	High-Impedance	L	L
FLOAT	X	High-Impedance	L	L

TYPICAL CHARACTERISTICS

If not specified, INPUT refers to non-inverting input

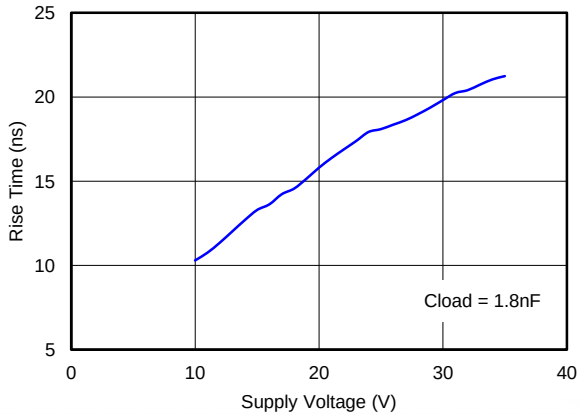


Figure 13. Rise Time vs. Supply Voltage

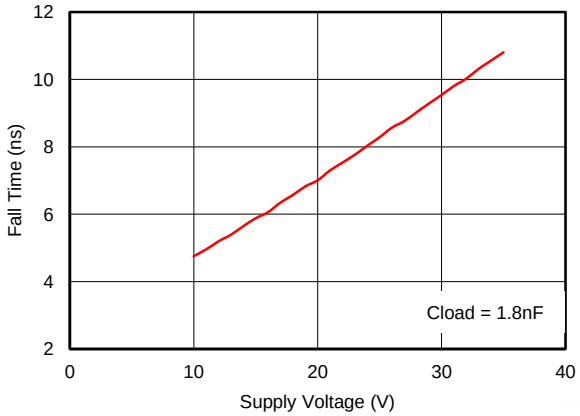


Figure 14. Fall Time vs. Supply Voltage

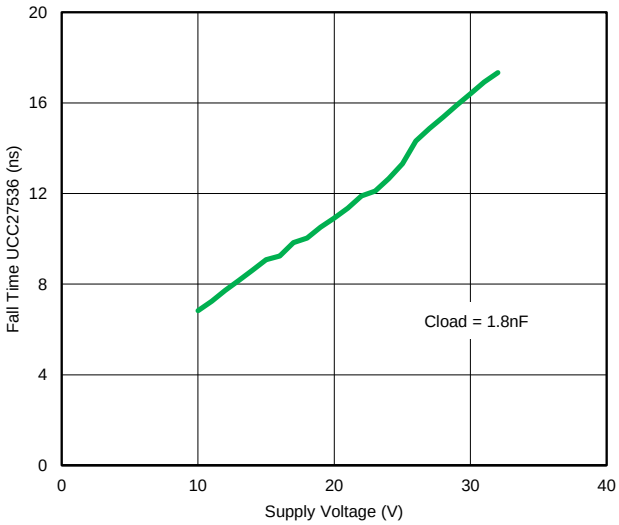


Figure 15. UCC27536 Fall Time vs. Supply Voltage

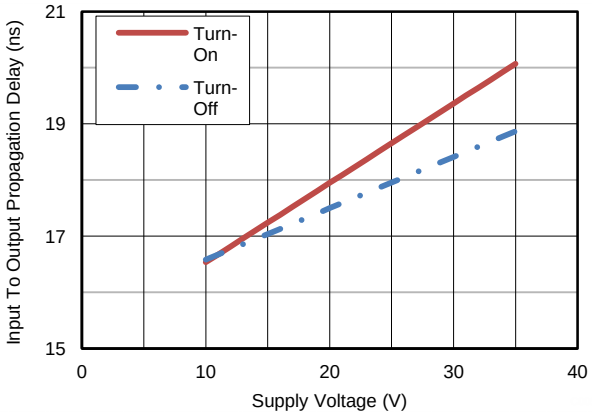


Figure 16. Propagation Delay vs. Supply Voltage

TYPICAL CHARACTERISTICS (continued)

If not specified, INPUT refers to non-inverting input

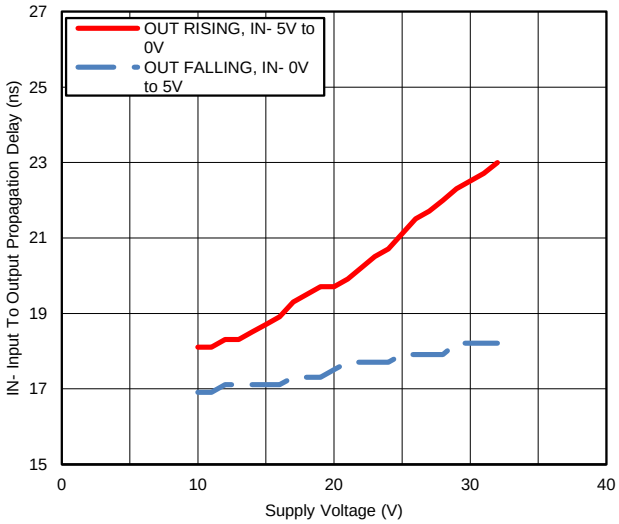


Figure 17. IN- Propagation Delay vs. Supply

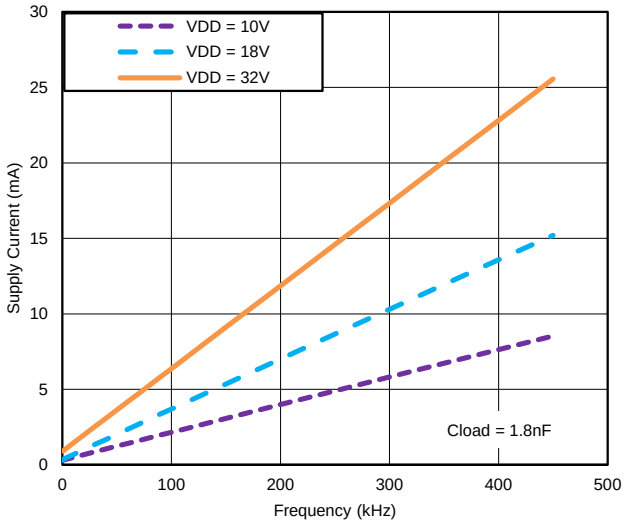


Figure 18. Operating Supply Current vs. Frequency

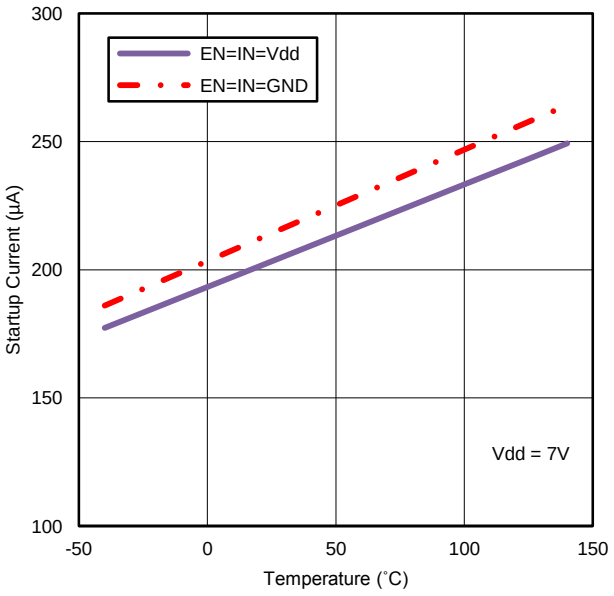


Figure 19. Start-Up Current vs. Temperature

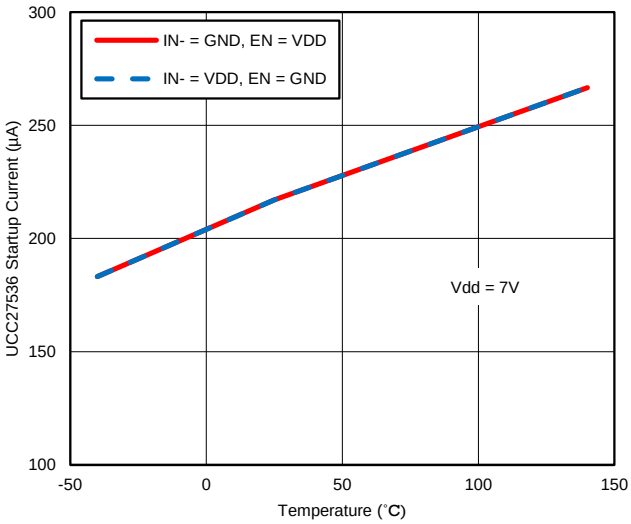


Figure 20. UCC27536 Start-Up Current vs. Temperature

TYPICAL CHARACTERISTICS (continued)

If not specified, INPUT refers to non-inverting input

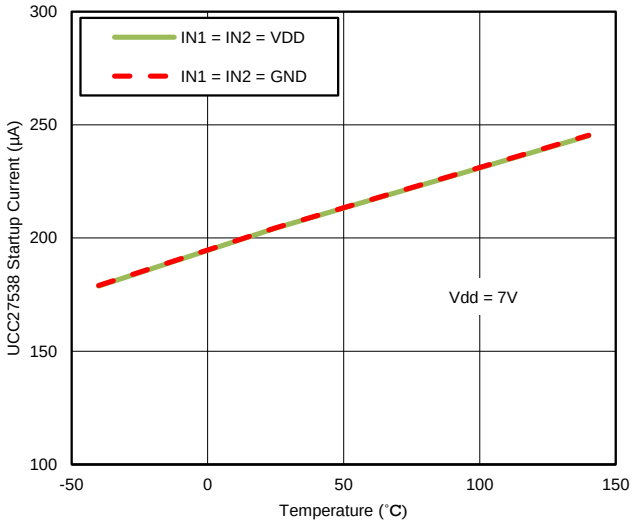


Figure 21. UCC27538 Start-Up Current vs. Temperature

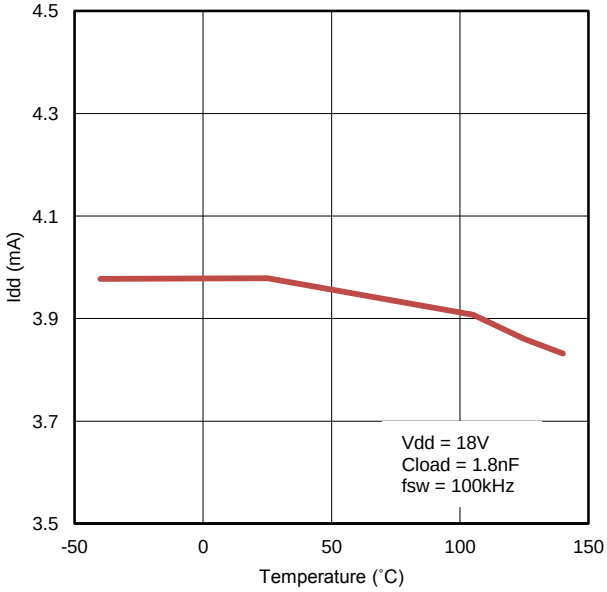


Figure 22. Operating Supply Current vs. Temperature (output switching)

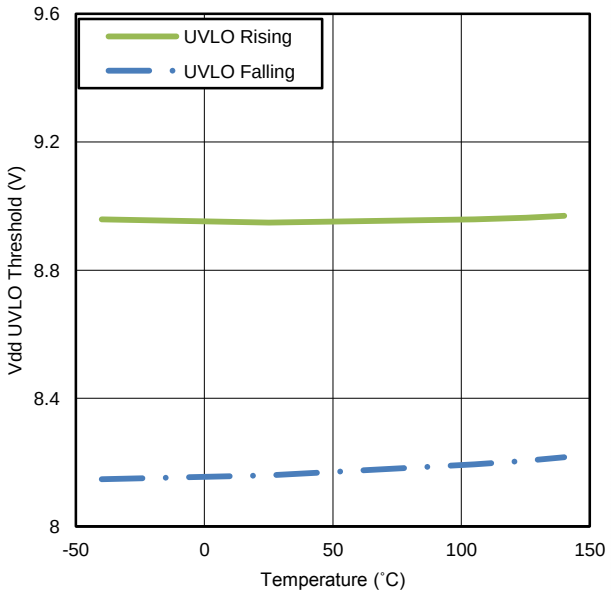


Figure 23. UVLO Threshold Voltage vs. Temperature

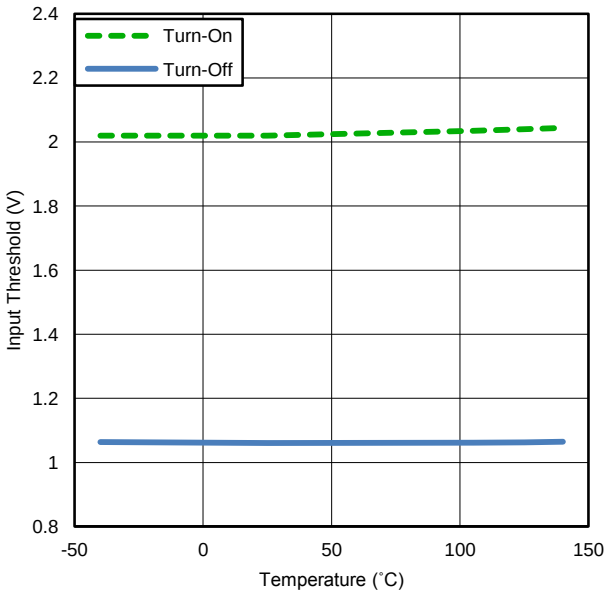


Figure 24. Input Threshold vs. Temperature

TYPICAL CHARACTERISTICS (continued)

If not specified, INPUT refers to non-inverting input

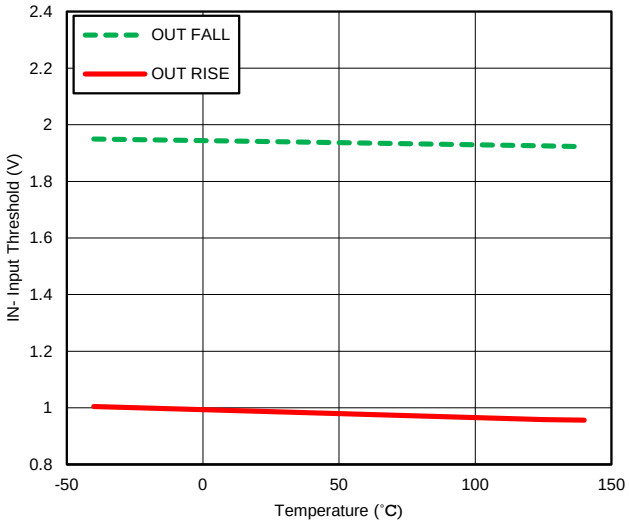


Figure 25. IN- Input Threshold vs. Temperature

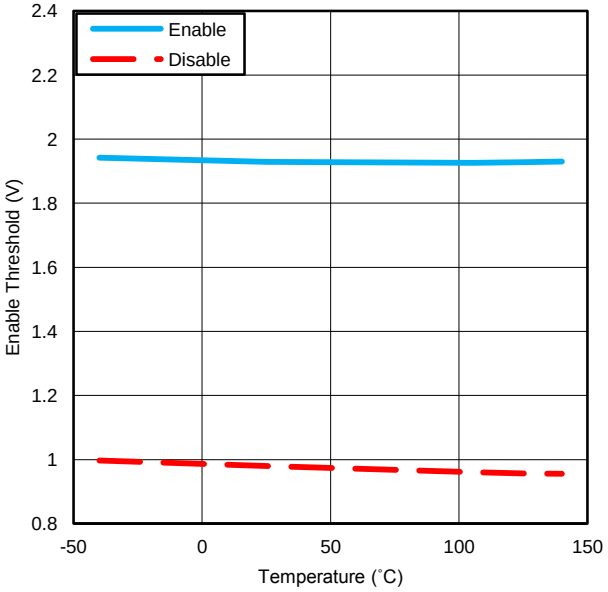


Figure 26. Enable Threshold vs. Temperature

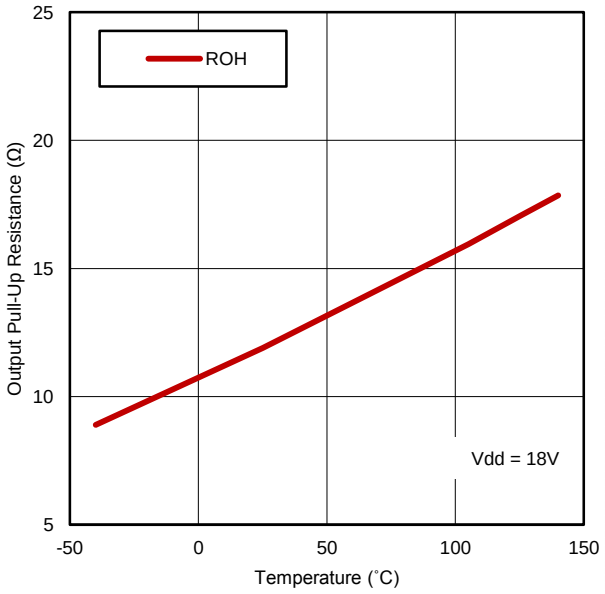


Figure 27. Output Pull-Up Resistance vs. Temperature

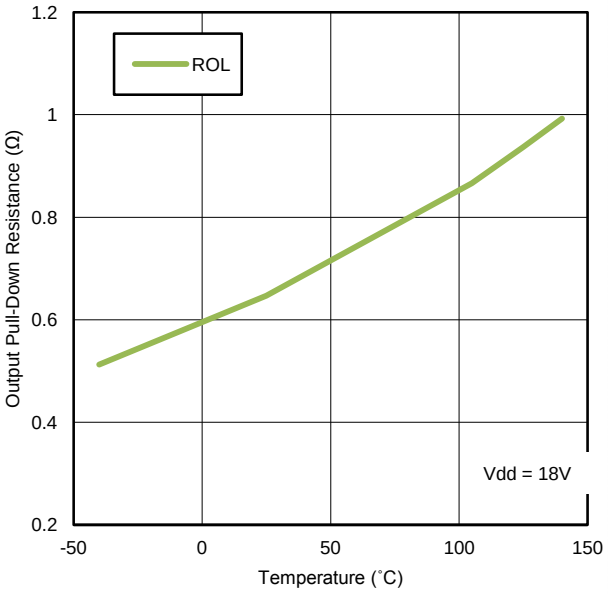


Figure 28. Output Pull-Down Resistance vs. Temperature

TYPICAL CHARACTERISTICS (continued)

If not specified, INPUT refers to non-inverting input

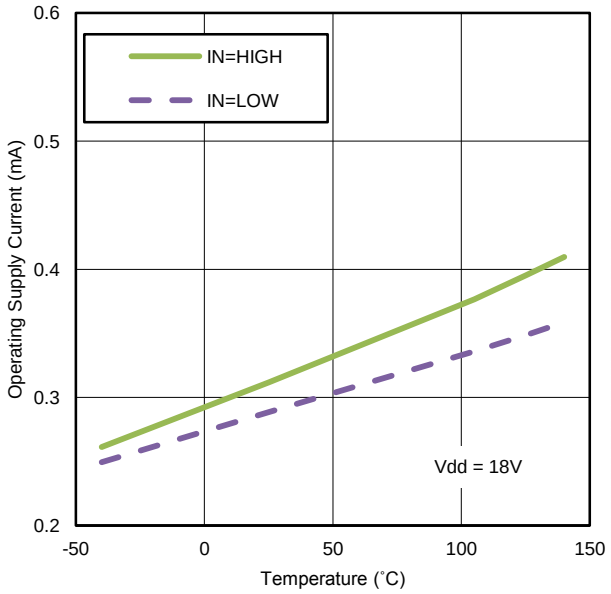


Figure 29. Operating Supply Current vs. Temperature (output in DC on/off condition)

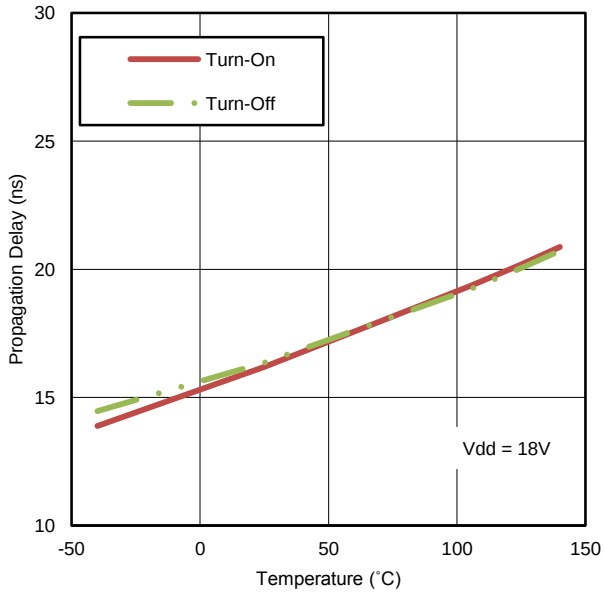


Figure 30. Input-to-Output Propagation Delay vs. Temperature

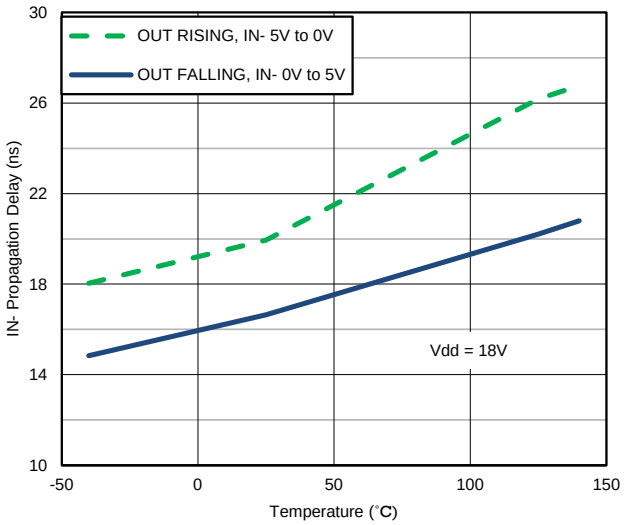


Figure 31. IN- Input-to-Output Propagation Delay vs. Temperature

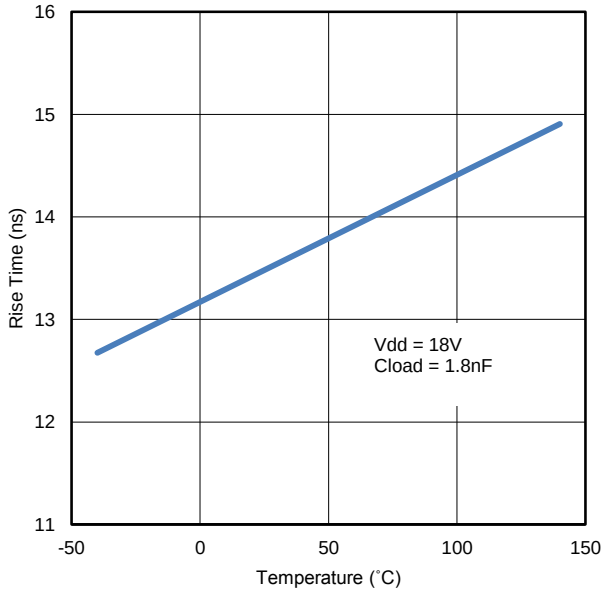


Figure 32. Rise Time vs. Temperature

TYPICAL CHARACTERISTICS (continued)

If not specified, INPUT refers to non-inverting input

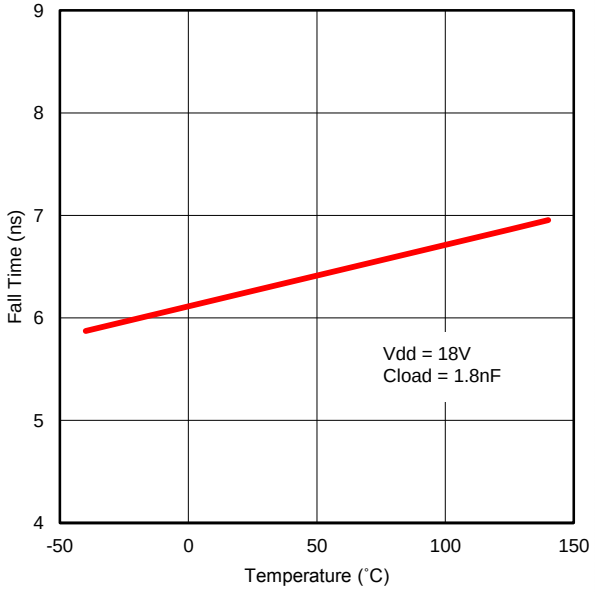


Figure 33. Fall Time vs. Temperature

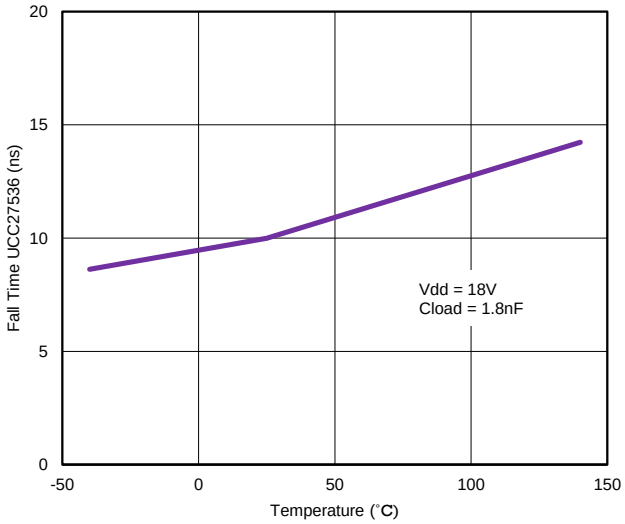


Figure 34. UCC27536 Fall Time vs. Temperature

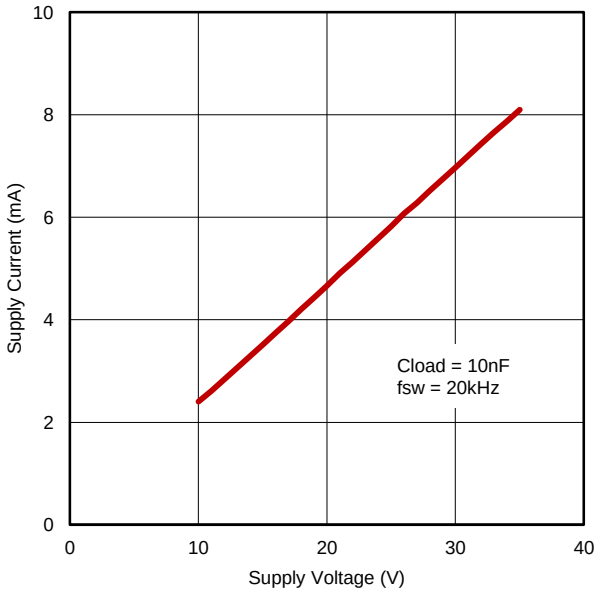


Figure 35. Operating Supply Current vs. Supply Voltage (output switching)

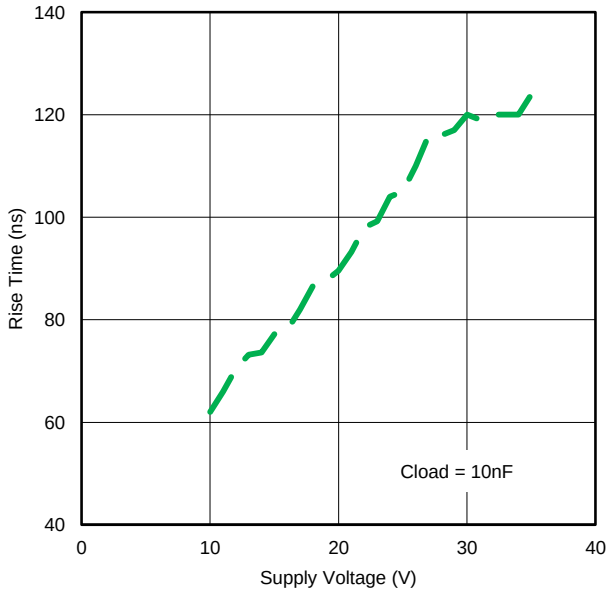


Figure 36. Rise Time vs. Supply Voltage

TYPICAL CHARACTERISTICS (continued)

If not specified, INPUT refers to non-inverting input

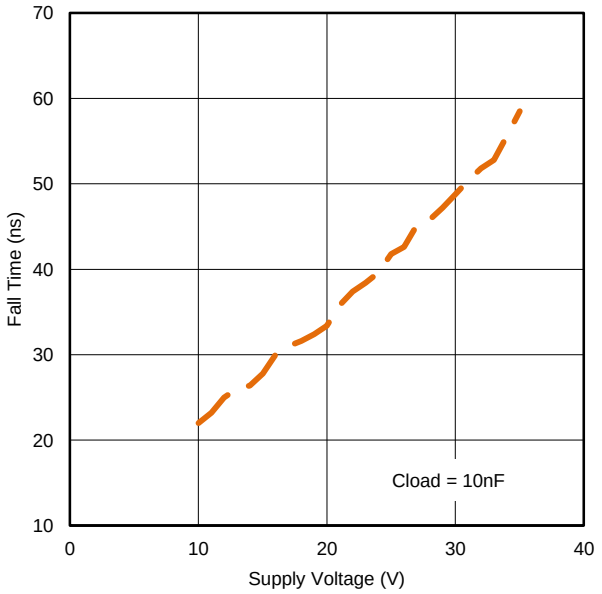


Figure 37. Fall Time vs. Supply Voltage

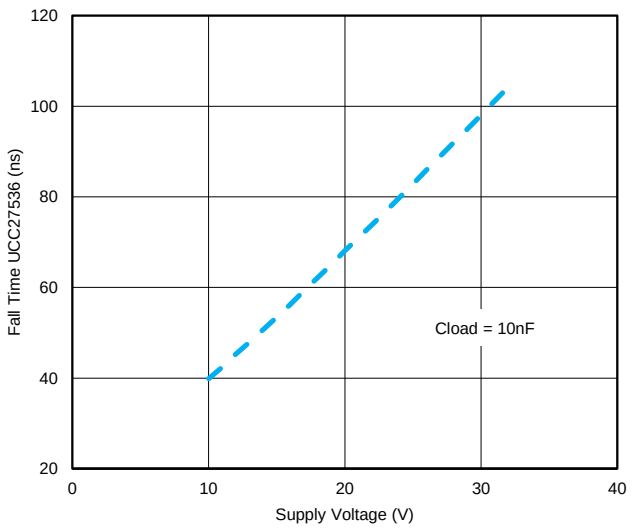


Figure 38. UCC27536 Fall Time vs. Supply Voltage

APPLICATION INFORMATION

High-current gate driver devices are required in switching power applications for a variety of reasons. In order to enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation will be often encountered since the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or p- n-channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this since they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC2753x is very flexible in this role with a strong current drive capability and wide supply voltage range up to 32 V. This allows the driver to be used in 12-V Si MOSFET applications, 20-V and -5-V (relative to Source) SiC FET applications, 15-V and -15-V(relative to Emitter) IGBT applications and many others. As a single-channel driver, the UCC2753x can be used as a low-side or high-side driver. To use as a low-side driver, the switch ground is usually the system ground so it can be connected directly to the gate driver. To use as a high-side driver with a floating return node however, signal isolation is needed from the controller as well as an isolated bias to the UCC2753x. Alternatively, in a high-side drive configuration the UCC2753x can be tied directly to the controller signal and biased with a non-isolated supply. However, in this configuration the outputs of the UCC2753x need to drive a pulse transformer which then drives the power-switch to work properly with the floating source and emitter of the power switch. Further, having the ability to control turn-on and turn-off speeds independently with both the OUTH and OUTL pins ensures optimum efficiency while maintaining system reliability. These requirements coupled with the need for low propagation delays and availability in compact, low-inductance packages with good thermal capability makes gate driver devices such as the UCC2753x extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design.

Table 2. UCC2753x Features and Benefits

FEATURE	BENEFIT
High source and sink current capability, 2.5 A and 5 A (asymmetrical).	High current capability offers flexibility in employing UCC2753x device to drive a variety of power switching devices at varying speeds.
Low 17 ns (typ) propagation delay.	Extremely low pulse transmission distortion.
Wide VDD operating range of 10 V to 32 V.	Flexibility in system design.
	Can be used in split-rail systems such as driving IGBTs with both positive and negative(relative to Emitter) supplies.
	Optimal for many SiC FETs.
VDD UVLO protection.	Outputs are held Low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down.
	High UVLO of 8.9V typical ensures that power switch is not on in high-impedance state which could result in high power dissipation or even failures.
Outputs held low when input pin (INx) in floating condition.	Safety feature, especially useful in passing abnormal condition tests during safety certification
Split output structure option (OUTH, OUTL).	Allows independent optimization of turn-on and turn-off speeds using series gate resistors.
Strong sink current (5 A) and low pull-down impedance (0.65 Ω).	High immunity to high dV/dt Miller turn-on events.
CMOS and TTL compatible input threshold logic with wide hysteresis.	Enhanced noise immunity, while retaining compatibility with microcontroller logic level input signals (3.3 V, 5 V) optimized for digital power.
Input capable of withstanding -6.5 V.	Enhanced signal reliability in noisy environments that experience ground bounce on the gate driver.

VDD Under Voltage Lockout

The UCC2753x device has internal under voltage lockout (UVLO) protection feature on the VDD pin supply circuit blocks. To ensure acceptable power dissipation in the power switch, this UVLO prevents the operation of the gate driver at low supply voltages. Whenever the driver is in UVLO condition (when VDD voltage less than V_{ON} during power-up and when VDD voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 8.9 V with 700-mV typical hysteresis. This hysteresis helps prevent chatter when low VDD supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at voltage levels such as 10 V to 32 V provides flexibility to drive Si MOSFETs, IGBTs, and emerging SiC FETs.

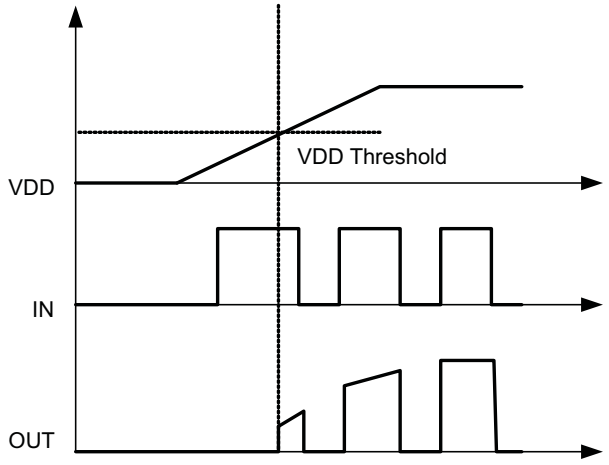


Figure 39. Power Up

Input Stage

The input pins of UCC2753x device are based on a TTL and CMOS compatible input threshold logic that is independent of the VDD supply voltage. With typical high threshold = 2 V and typical low threshold = 1 V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3-V or 5-V logic. Wider hysteresis (typically 1 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. This device also features tight control of the input pin threshold voltage levels which eases system design considerations and guarantees stable operation across temperature. The very low input capacitance , typically 20 pF, on these pins reduces loading and increases switching speed.

The device features an important safety function wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved using pull-up or pull-down resistors on the input pins as shown in the block diagrams.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a separate daughter board or PCB layout has long input connection traces:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. Since the device features just one GND pin which may be referenced to the power ground, this may interfere with the differential voltage between Input pins and GND and trigger an unintended change of output state. Because of fast 17 ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage
- 1-V Input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

If limiting the rise or fall times to the power device to reduce EMI is necessary, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

Finally, because of the unique input structure that allows negative voltage capability on the Input and Enable pins, caution must be used in the following applications:

- Input or Enable pins are switching to amplitude > 15 V
- Input or Enable pins are switched at dV/dt > 2 V/ns

If both of these conditions occur, it is advised to add a series 150-Ω resistor for the pin(s) being switched to limit the current through the input structure.

Enable Function

The Enable (EN) pin of the UCC2753x has an internal pull-up resistor to an internal reference voltage so leaving Enable floating turns on the driver and allows it to send output signals properly. If desired, the Enable can also be driven by low-voltage logic to enable and disable the driver.

Output Stage

The output stage of the UCC2753x device is illustrated in Figure 40. The UCC2753x device features a unique architecture on the output stage which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turn-on transition (when the power switch drain/collector voltage experiences dV/dt). The device output stage features a hybrid pull-up structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate driver device is able to deliver a brief boost in the peak sourcing current enabling fast turn on.

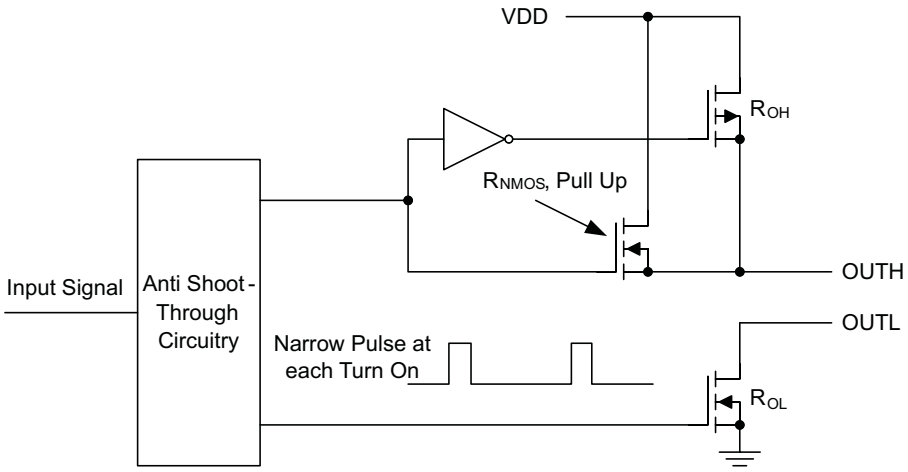


Figure 40. UCC27531 Gate Driver Output Stage

Split output depicted in Figure 40. For devices with single OUT pin, OUTH and OUTL are connected internally and then connected to OUT.

The R_{OH} parameter (see Electrical Table) is a DC measurement and it is representative of the on-resistance of the P-Channel device only, since the N-Channel device is turned-on only during output change of state from low to high. Thus the effective resistance of the hybrid pull-up stage is much lower than what is represented by ROH parameter. The pull-down structure is composed of a N-Channel MOSFET only. The ROL parameter (see ELECTRICAL CHARACTERISTICS), which is also a DC measurement, is representative of true impedance of the pull-down stage in the device. In UCC2753x, the effective resistance of the hybrid pull-up structure is approximately 3 x R_{OL}.

The UCC2753x is capable of delivering 2.5-A source, and up to 5-A sink at VDD = 18 V. Strong sink capability results in a very low pull-down impedance in the driver output stage which boosts immunity against the parasitic Miller turn-on (high slew rate dV/dt turn on) effect that is seen in both IGBT and FET power switches .

An example of a situation where Miller turn on is a concern is synchronous rectification (SR). In SR application, the dV/dt occurs on MOSFET drain when the MOSFET is already held in Off state by the gate driver. The current charging the C_{GD} Miller capacitance during this high dV/dt is shunted by the pull-down stage of the driver. If the pull-down impedance is not low enough then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turn on. This phenomenon is illustrated in Figure 41.

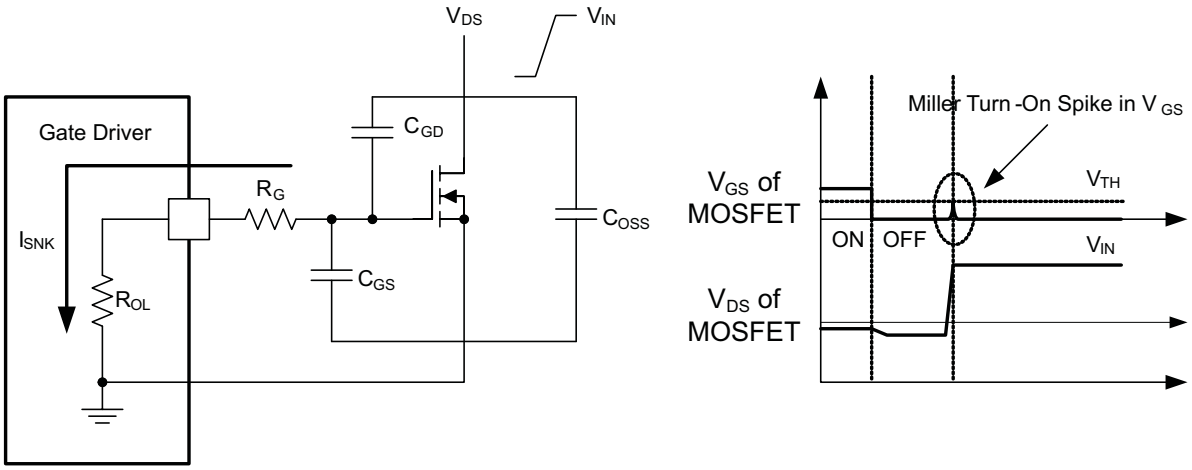


Figure 41. Low Pull-Down Impedance in UCC2753x (output stage mitigates Miller turn-on effect)

The driver output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS output stage which delivers very low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky diode clamps may be eliminated.

Power Dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

The DC portion of the power dissipation is $P_{DC} = I_Q$ x VDD where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections etc and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through). The UCC2753x features very low quiescent currents (less than 1 mA) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible. In practice this is the power consumed by driver when its output is disconnected from the gate of power switch.

The power dissipated in the gate driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2$$

where

- C_{LOAD} is load capacitor and V_{DD} is bias voltage feeding the driver. (2)

There is an equal amount of energy dissipated when the capacitor is discharged. During turn off the energy stored in capacitor is fully dissipated in drive circuit. This leads to a total power loss during switching cycle given by the following:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw}$$

where

- f_{SW} is the switching frequency (3)

The switching load presented by a power FET and IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence, $Q_g = C_{LOAD} V_{DD}$, to provide the following equation for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw} = Q_g V_{DD} f_{sw} \quad (4)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET and IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET and IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{sw} \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right)$$

where

- $R_{OFF} = R_{OL}$ and R_{ON} (effective resistance of pull-up structure) = 3 x R_{OL} (5)

Thermal Information

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the 'Thermal Information' section of the datasheet. For detailed information regarding the thermal information table, please refer to Application Note from Texas Instruments entitled "IC Package Thermal Metrics" (SPRA953A).

PCB Layout

Proper PCB layout is extremely important in a high current, fast switching circuit to provide appropriate device operation and design robustness. The UCC2753x gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak current capability is even higher (2.5-A and 5-A peak current is at VDD = 18 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the driver Output pins and the gate of the power switch device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD during turn-on of power switch. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (driver device, power switch and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances – during turn-on and turn-off transients, which induces significant voltage transients on the output pins of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces of a current loop, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller etc at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

REVISION HISTORY

Changes from Original (December 2012) to Revision A	Page
• Changed Block Diagram.	7

Changes from Revision A (December 2012) to Revision B	Page
• Added UCC27533, UCC27536, UCC27537 and UCC27538 parts to the datasheet.	1

Changes from Revision B (April 2013) to Revision C	Page
• Added additional DESCRIPTION information.	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UCC27531DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7531	Samples
UCC27531DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7531	Samples
UCC27533DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7533	Samples
UCC27533DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	7533	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

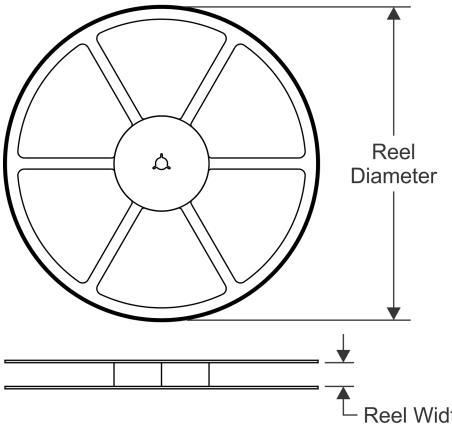
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

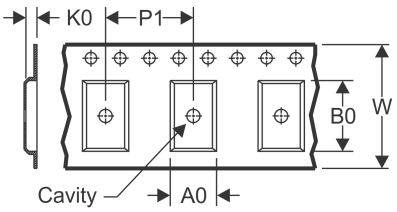
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

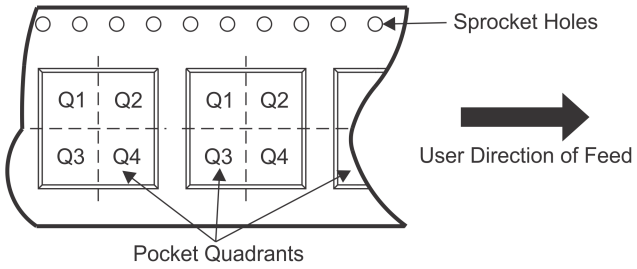


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

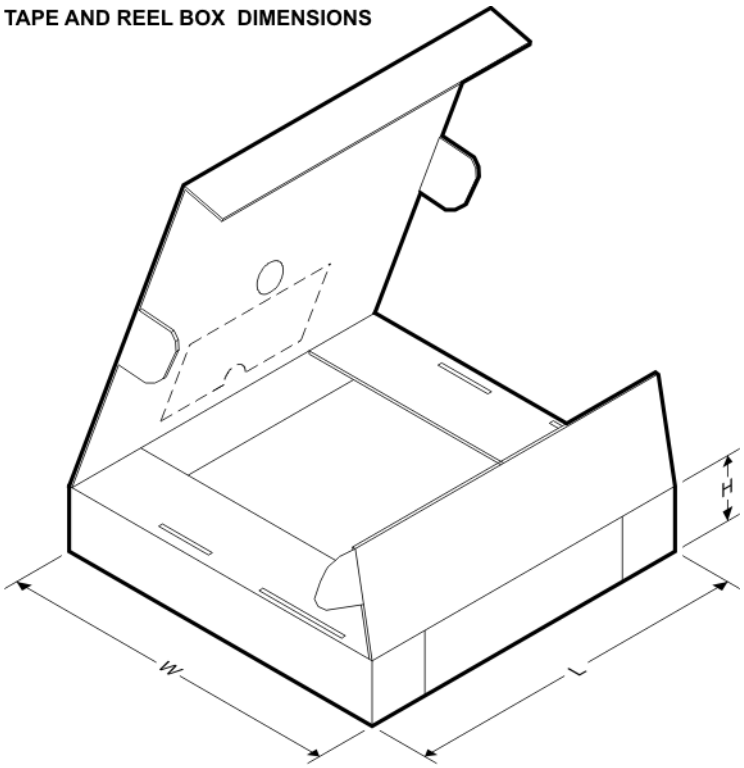
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27531DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27531DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27533DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27533DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

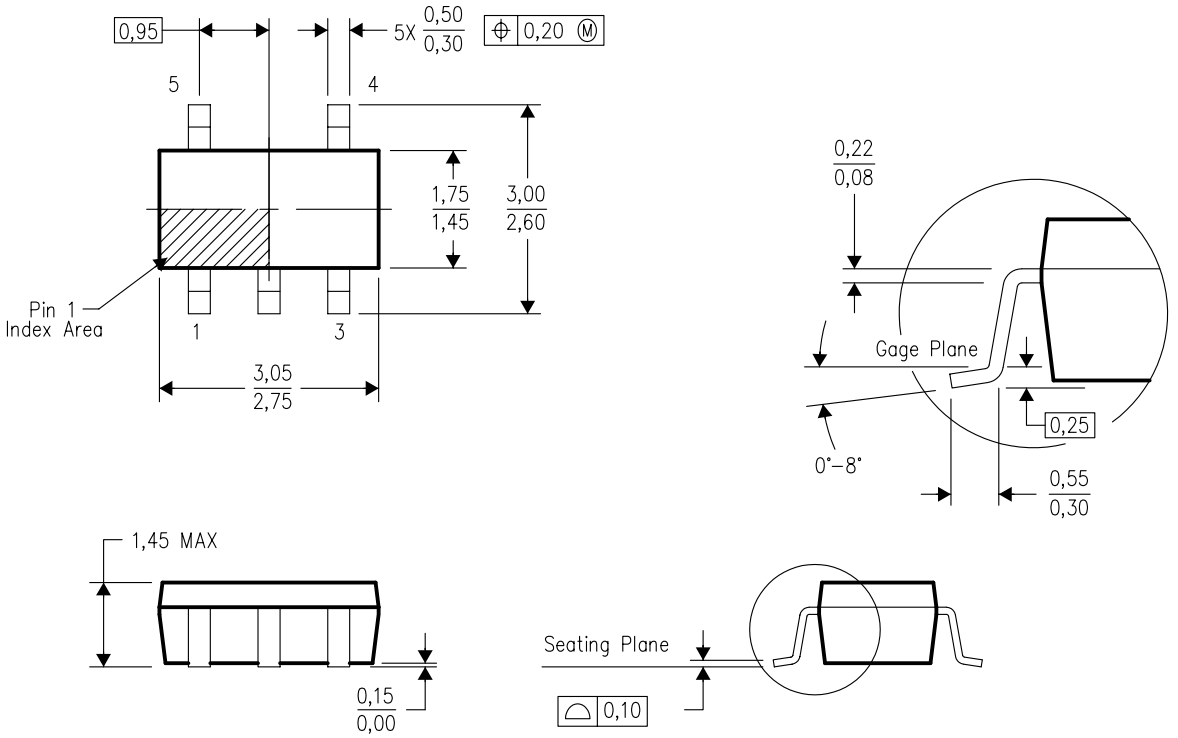
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27531DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
UCC27531DBVT	SOT-23	DBV	6	250	203.0	203.0	35.0
UCC27533DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0
UCC27533DBVT	SOT-23	DBV	5	250	203.0	203.0	35.0

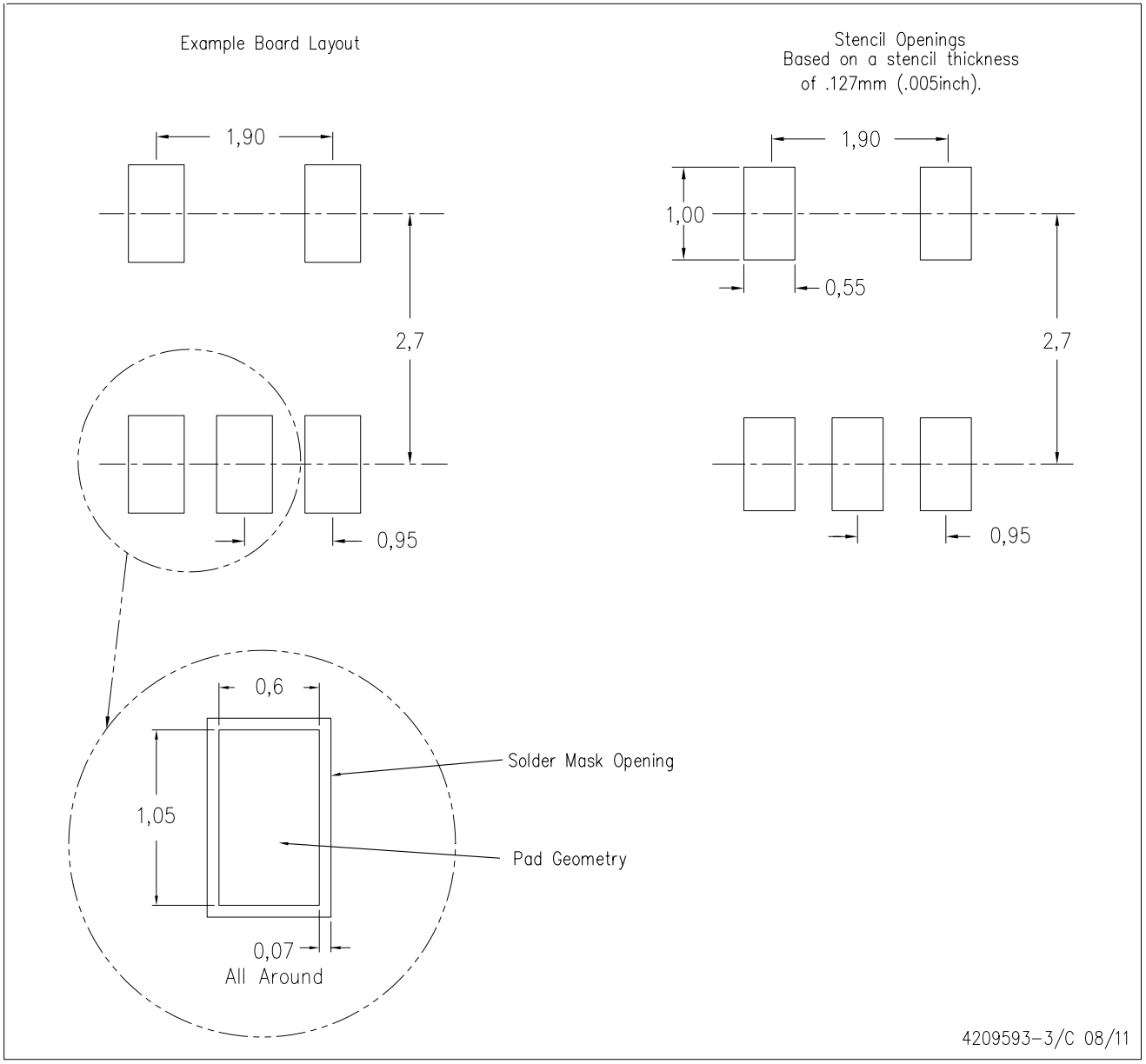
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

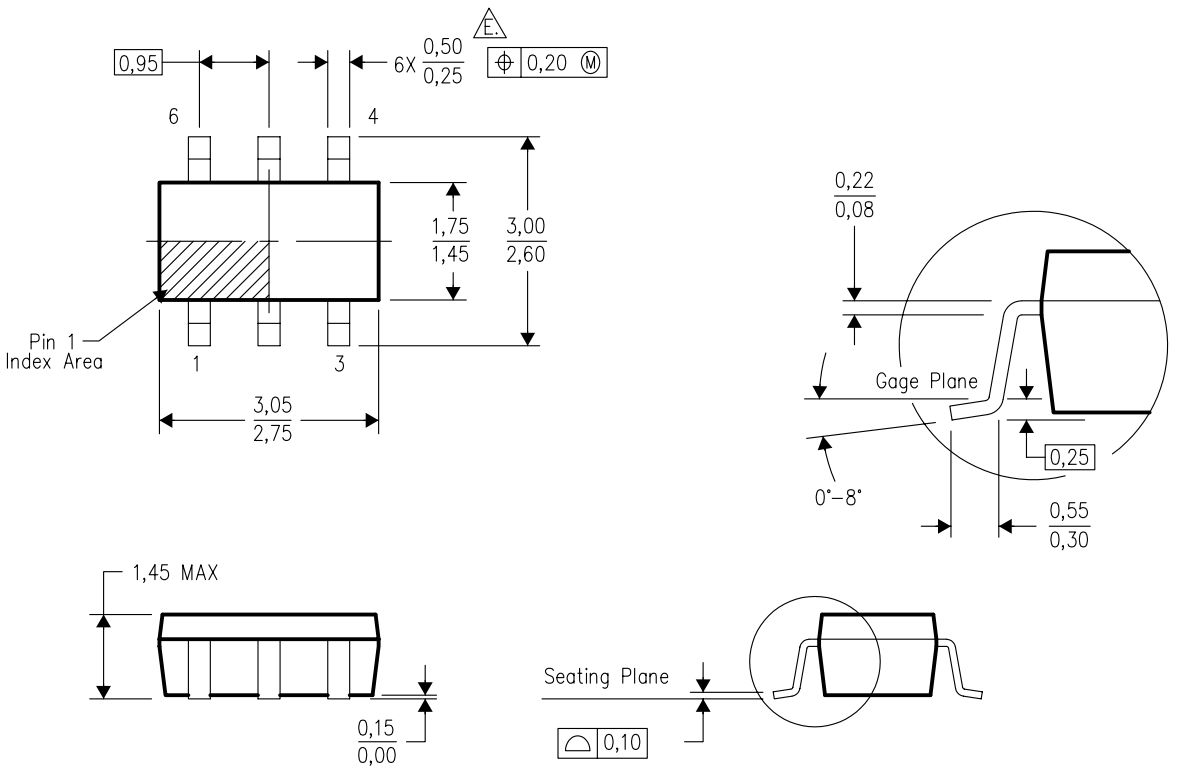
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

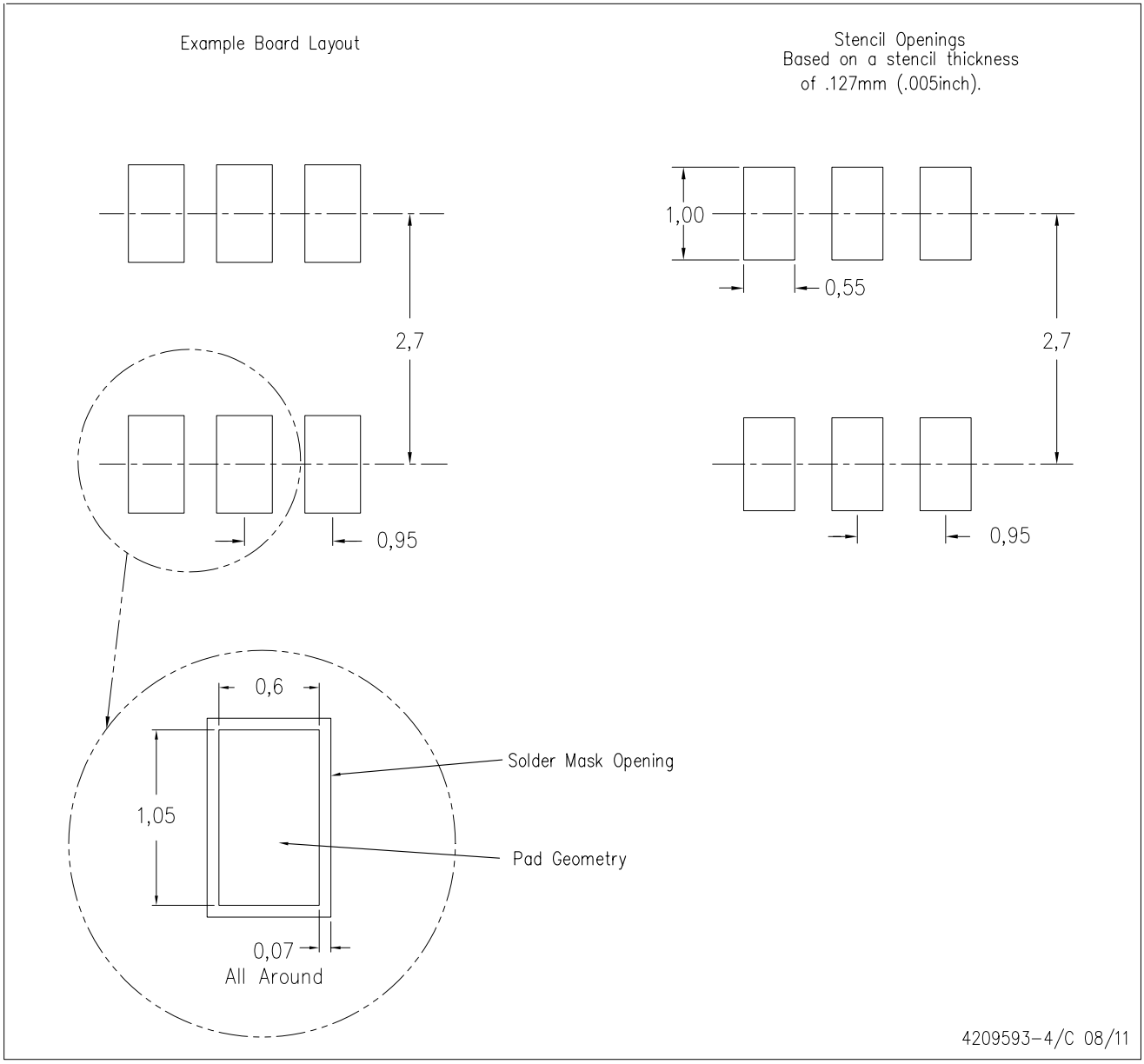
DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4073253–5/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

DBV (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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